Notice of Allowability	Application No.	Applicant(s)	
	10/621,504	MALLINSON, MARTIN	
	Examiner	Art Unit	
	Andrew C. Flanders	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the phone conversation with Ernest Beffel on 07 March 2006*.

2. ☒ The allowed claim(s) is/are *2,3,5-23,25-46,49-53 and 55-85*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Ernest Beffel on 07 March 2006.

The application has been amended as follows:

1. (cancelled)

2. (currently amended) ~~The signal processor of claim 1, further comprising~~
A signal processor, comprising:
a pulse width modulator having a clock rate;
a digital filter configured to receive an output of said pulse width modulator, wherein said output comprises a distortion, and wherein said digital filter samples said output at said clock rate to suppress said distortion; and
an oversampling modulator upstream of and coupled to said pulse width modulator.

3. (original) The signal processor of claim 2, wherein said oversampling modulator comprises a sigma-delta type modulator.

4. (cancelled)

5. (previously presented) The signal processor of claim 3, wherein said oversampling modulator generates an oversampled signal having a period and a total number of levels, and wherein said clock rate is at least M times said period, where M is said total number of levels in said oversampled signal.

6. (original) The signal processor of claim 5, wherein said sigma-delta type modulator comprises a first order sigma-delta type modulator.

7. (previously presented) The signal processor of claim 3, further comprising a filter upstream of said pulse width modulator.

8. (currently amended) The signal processor of claim [[1]] 2, wherein said digital filter comprises an IIR filter.

9. (original) The signal processor of claim 8, wherein said IIR filter comprises a single pole filter.

10. (currently amended) The signal processor of claim [[1]] 2, wherein said digital filter comprises a low pass filter.

11. (currently amended) ~~The signal processor of claim 1, further comprising~~ A signal processor, comprising:

a pulse width modulator having a clock rate;

a digital filter configured to receive an output of said pulse width modulator, wherein said output comprises a distortion, and wherein said digital filter samples said output at said clock rate to suppress said distortion; and

a feedback path comprising said digital filter.

12. (currently amended) An integrated circuit chip system comprising the signal processor of claim [[1]] 2.

13. (original) The integrated circuit chip system of claim 12, wherein said system provides a two-channel output.

14. (original) The integrated circuit chip system of claim 12, wherein said system provides an eight-channel output.

15. (currently amended) A portable audio player comprising the signal processor of claim [[1]] 2.

16. (original) The portable audio player of claim 15, further comprising a digital audio signal source.

17. (previously presented) The portable audio player of claim 15, wherein said digital audio source comprises a memory medium reader.

18. (original) The portable audio player of claim 17, wherein said memory medium reader comprises an optical disk reader.

19. (original) The portable audio player of claim 16, wherein said digital audio signal source comprises a memory for storage of a digital audio file.

20. (original) The portable audio player of claim 16, wherein said digital audio signal source comprises a digital receiver.

21. (original) An audio power amplification system comprising the signal processor of claim [[1]] 2.

22. (previously presented) The audio power amplification system of claim 21, further comprising an RC type demodulation filter.

23. (original) A digital circuit for suppressing a distortion in a digital signal that exists after a pulse width modulation, wherein said pulse width modulation occurs at a clock rate, and wherein said digital circuit comprises a digital filter configured to receive said signal having said distortion and to sample said signal at said clock rate to suppress said distortion.

24. (cancelled)

25. (currently amended) ~~The digital signal processing circuit of claim 24, further comprising~~

A digital signal processing circuit, comprising:

a pulse width modulator having an output with a distortion; and

means for sampling said output and suppressing said distortion in a digital domain; and

an oversampling modulator coupled to the input of the pulse width modulator.

26. (original) The digital signal processing circuit of claim 25, wherein said oversampling modulator comprises a sigma-delta type modulator.

27. (original) The digital signal processing circuit of claim 26, wherein said sigma-delta type modulator comprises a first order sigma-delta type modulator.

28. (original) The digital signal processing circuit of claim 25, wherein said oversampling modulator is upstream of said pulse width modulator.

29. (previously presented) The digital signal processing circuit of claim 28, wherein said oversampling modulator generates an oversampled signal having a period and a total number of levels, and said pulse width modulator operates at a clock rate that is at least M times said period, where M is said total number of levels in said oversampled signal.

30. (previously presented) The digital signal processing circuit of claim 25, further comprising a filter upstream of said pulse width modulator.

31. (currently amended) An integrated circuit chip system comprising the signal processor of claim [[24]] 25.

32. (original) The integrated circuit chip system of claim 31, wherein said system provides a two-channel output.

33. (original) The integrated circuit chip system of claim 31, wherein said system provides an eight-channel output.

34. (currently amended) An audio power amplification system comprising the signal processor of claim [[24]] 25.

35. (original) The audio power amplification system of claim 34, further comprising an RC type demodulation filter.

36. (currently amended) A portable audio player comprising the signal processor of claim [[24]] 25.

37. (original) The portable audio player of claim 36, further comprising a digital audio signal source.

38. (original) The portable audio player of claim 37, wherein said digital audio signal source comprises a memory medium reader.

39. (original) The portable audio player of claim 38, wherein said memory medium reader comprises an optical disk reader.

40. (original) The portable audio player of claim 37, wherein said digital audio signal source comprises a memory for storage of a digital audio file.

41. (original) The portable audio player of claim 37, wherein said digital audio signal source comprises a digital receiver.

42. (currently amended) The digital signal processing circuit of claim [[24]] 25, wherein said sampling occurs at a clock rate of said pulse width modulator.

43. (previously presented) A signal processor for modulating a digital input signal, comprising a closed loop digital circuit comprising:

a forward path comprising a first filter stage coupled with and upstream from an encoder stage, wherein said encoder stage comprises a first order sigma-delta type modulator and a pulse width modulator, wherein said sigma-delta type modulator generates an oversampled signal having a period and a total number of levels, and said pulse width modulator operates at a clock rate that is at least M times said period, where M is said total number of levels in said oversampled signal, and wherein said forward path produces an output having a distortion; and

a feedback path comprising a digital filter that samples said output in a digital domain to suppress said distortion.

44. (original) The signal processor of claim 43, wherein said digital filter samples said output at said clock rate.

45. (original) The signal processor of claim 43, wherein said signal processor exhibits a modulation depth of up to about –1 db in an audio frequency band.

46. (original) The signal processor of claim 43, wherein said signal processor reduces a total harmonic distortion to about 90 – 100 db.

47. (canceled).

48. (cancelled)

49. (currently amended) A method, comprising:

modulating a first pulse code modulated signal having a first resolution <u>using a sigma-delta type modulator</u> into a second pulse code modulated signal having a second resolution, wherein said second resolution is smaller than said first resolution;

modulating said second pulse code modulated signal into a third signal comprising a plurality of pulses in time having a clock rate; and

filtering in a digital domain said plurality of pulses in time to suppress a distortion in said third signal.

50. (original) The method of claim 49, wherein said first resolution is between 12 bits and 24 bits inclusively.

51. (original) The method of claim 50, wherein said first resolution is 16 bits.

52. (original) The method of claim 50, wherein said second resolution is between 2 bits and 6 bits inclusively.

53. (original) The method of claim 52, wherein said second resolution is 4 bits.

54. (cancelled)

55. (original) The method of claim [[54]] 49, wherein said sigma-delta type modulator is a first order sigma-delta type modulator.

56. (original) The method of claim 49, wherein said modulating said second pulse code modulated signal comprises using a pulse width modulator.

57. (original) The method of claim 49, wherein said filtering comprises using a digital filter.

58. (original) The method of claim 57, wherein said digital filter comprises an IIR filter.

59. (original) The method of claim 58, wherein said IIR filter comprises a single pole filter.

60. (original) The method of claim 57, wherein said digital filter comprises a low pass filter.

61. (original) The method of claim 49, wherein said filtering comprises forming a feedback signal having said first resolution.

62. (original) The method of claim 49, wherein said plurality of pulses in time is a substantially small range of pulses in time.

63. (previously presented) The method of claim 49, wherein said modulating said first pulse code modulated signal comprises generating an oversampled signal having a period and a total number of levels, wherein said modulating said second pulse code modulated digital signal occurs at a clock rate that is at least M times said period, where M is said total number of levels in said oversampled signal.

64. (original) The method of claim 49, wherein said filtering comprises sampling at said clock rate.

65. (original) The method of claim 49, further comprising amplifying said third signal to produce an amplified output.

66. (original) The method of claim 65, further comprising creating an analog signal from said amplified output.

67. (original) The method of claim 66, wherein said creating comprises using an RC filter circuit.

68. (currently amended) A device, comprising:

means for modulating a first pulse code modulated signal having a first resolution using a sigma-delta type modulator into a second pulse code modulated signal having a second resolution, wherein said second resolution is smaller than said first resolution;

means for modulating said second pulse code modulated signal into a third signal comprising a plurality of pulses in time having a clock rate; and

means for filtering in a digital domain said plurality of pulses in time to suppress a distortion in said third signal.

69. (previously presented) The signal processor of claim 7, wherein the filter is an integrator.

70. (previously presented) The digital signal processing circuit of claim 30, wherein the filter is an integrator.

71. (previously presented) The signal processor of claim 43, wherein said signal processor exhibits a modulation depth of up to about 0 db in an audio frequency band.

72. (previously presented) The signal processor of claim 43, wherein said signal processor reduces a total harmonic distortion to about 90 – 140 db.

73. (previously presented) The method of claim 49, wherein said first resolution is between 12 bits and 24 bits inclusively.

74. (currently amended) A loop that corrects distortion caused by transforming an oversampled pulse code modulated signal to a pulse width modulated signal, including;

a wide-bit input signal;

a difference element accepting the wide-bit input signal;

an input filter coupled to the difference element;

an oversampler coupled to the input filter, producing an oversampled signal having less precision and higher frequency than the wide-bit signal;

a pulse width modulator coupled to the oversampler;

an output coupled to the pulse width modulator; and

a digital feedback filter coupled to the pulse width modulator, the digital feedback filter

producing a correction signal that at least partially compensates for undesired distortion introduced by the pulse width modulator,

~~formating~~ formatting the correction signal to match precision and frequency of the wide-bit input signal and

feeding back the formatted correction signal to the difference element.

75. (previously presented) The loop of claim 74, wherein the summing element calculates a difference between the wide-bit input signal and the formatted correction signal.

76. (previously presented) The loop of claim 74, wherein input filter is an integrator.

77. (previously presented) The loop of claim 74, wherein input filter is a second order element of the oversampler.

78. (previously presented) The loop of claim 74, wherein the digital feedback filter is a single pole IIR filter.

79. (previously presented) The loop of claim 74, wherein the digital feedback filter is an integrator.

80. (previously presented) The loop of claim 74, wherein the digital feedback filter is a recursive averager.

81. (previously presented) The loop of claim 74, wherein the oversampler is a sigma delta modulator.

82. (previously presented) A method of preprocessing a pulse encoded digital signal for amplification by a digital amplifier, the method including:

oversampling a wide-bit input signal to produce a second signal that has lower bits precision than the input signal;

converting the second signal into a pulse width modulated signal, whereby undesirable distortion is introduced;

digitally filtering the pulse width modulated signal to correct at least part of the undesirable distortion and produce a correction signal; and

producing a corrected pulse width modulated signal using the correction signal combined with a version of the input signal.

83. (previously presented) The method of claim 82, further including:

formatting the correction signal to match bit-width and frequency of the input signal;

feeding back the formatted correction signal and filtering it together with the input signal.

84. (previously presented) The method of claim 83, wherein an integrator is used to filter the formatted correction signal together with the input signal.

85. (previously presented) The method of claim 82, wherein the input signal has about 12 to 24 bits precision per sample.

The following is an examiner's statement of reasons for allowance:

Applicant has rewritten previously indicated allowable subject matter (from the previous action) into the claims.

Claims 2, 25, 43, 49, 68, 74 and 82 claim an oversampling modulator upstream of and coupled to said pulse width modulator. Neither Midya nor Oprescu discloses this limitation. Ruha discloses an oversampling modulator upstream of a pulse width modulator (Fig. 4) and Masuda discloses one as well (Fig. 4). However, it would not have been obvious to one of ordinary skill in the art to apply the teachings of Masuda or Ruha to add an oversampling modulator to the circuits disclosed by Midya and Oprescu as there are no disclosed advantages for using one nor was the knowledge known in the art to use one.

In most of the art found with the inclusion of an oversampling modulator upstream of a pulse width modulator, the art is generally unconcerned with correcting the output of a PWM. Masuda (U.S. Patent Application Publication 2002/0105377) discloses a sigma delta oversampling modulator upstream of a PWM (Fig. 4) for the purpose of compressing the number of bits. Masuda is completely silent as to whether there is noise in the output of the pulse width modulator or any way to correct this. Ruha states that the output of the PWM is assumed to be ideal. In most of the similar art, the noise is generated at the switching stage (see paragraph 42 of Masuda and

element 14 of Ruha). Both of these inventions are geared to correct the noise in the switching stage, not the PWM.

Correction of noise in a pulse signal such as the cited art in the previous action Oprescu (U.S. Patent 6,208,279) and Midya (6,504,427) is known as well. Both of these sources correct the output of a pulse forming stage using a digital filter. Neither, however, teach an oversampling modulator upstream. Oversampling in DSP is often done in order to preserve a signal by sampling higher than the Nyquist Rate. The signals in Midya and Oprescu are already sampled. Sampling them at a higher rate would not produce a signal with any further desirable features. Thus, as there is no motivation given in any of the references and there is no apparent advantage that was well known at the time of the invention, the claims are determined to contain allowable subject matter.

Claims 11 discloses the signal processor further comprising a feedback path comprising said digital filter. As shown above correction of noise in a pulse signal such as the cited art in the previous action Oprescu (U.S. Patent 6,208,279) and Midya (6,504,427) is known. Both of these sources correct the output of a pulse forming stage using a digital filter. Neither, however, explicitly disclose the claimed digital filter in feedback loop. Feedback paths are notoriously well known in the art. The general purpose of a feedback loop is to create a system that is more stable. Implementing one in the however, would not provide a system of any increased stability nor would it have added any apparent advantages over the prior art. Thus, as there is no motivation given

in any of the references and there is no apparent advantage that was well known at the time of the invention, the claim are determined to contain allowable subject matter.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew C. Flanders whose telephone number is (571) 272-7516. The examiner can normally be reached on M-F 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on (571) 272-7546. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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